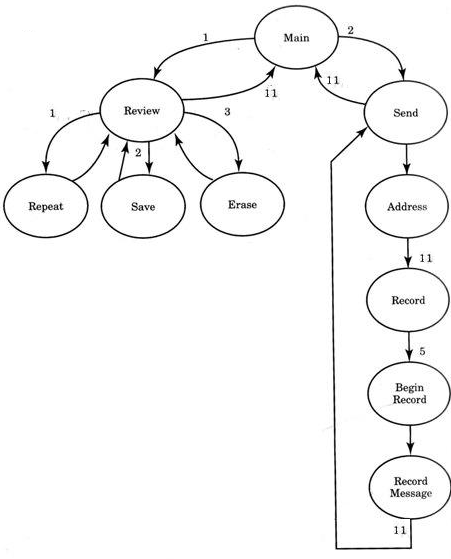
Tutorial

1. Write a VHDL code for the state machine diagram shown as in **Figure 1**. In your code, declare ‘package’ called vm\_pack to declare the ‘type’ for the state. The signal output for the design is shown in **Table 1**.



**Figure 1:** State Machine to control voice mail

|  |  |
| --- | --- |
| **State** | **Output** |
| repeat\_st | play=1 |
| save\_st | save=1 |
| erase\_st | erase=1 |
| address\_st | address =1 |
| begin\_rec\_st | recrd=1 |
| message\_st | recrd =1 |

**Table 1:** Output for state machine

1. Create a state machine VHDL program for the following diagram. R, Y and G are the outputs, a is the input and st\_ is the states. In your code, declare ‘package’ called vm\_pack to declare the ‘type’ for the state.

